COLUMBIA | ENGINEERING
The Fu Foundation School of Engineering and Applied Science

Welcome to ELEN E3106/4106!
(Advanced) Solid State Devices and Materials

- **Time:** Tuesday, Thursday 11:40am - 12:55pm
- **Location:** 417 International Affairs Building
- **Credits:** 3.5 for 3106, 3 for 4106
- **Instructor:** Prof. Savannah Eisner (savannah.eisner@columbia.edu)
- **TA:** Ethan Liu
- **CA/Grader:** Akanksha Sahoo, Sunny Hu
- **Office Hours:**
  - Prof. Eisner: Mondays 2-3pm, Mudd Building, 1328 13th floor
  - TA: Friday 11:30-12:30pm and TBD

This class is about…

The physics and basic operating principles of a number of common solid state electronic devices including:

- p-n and M-S Junctions
- Light-Emitting Diodes/Photodetectors
- Field Effect Transistors FET
- MOS Capacitor
- Bipolar Junction Transistors BJT

Course Goals

- To obtain a solid foundation in semiconductor devices
- Gain exposure to important applications for devices
- To prepare for more advanced classes and provide background for research in semiconductor devices

Suitability

- This class is suitable for EE and other STEM majors who have an undergrad level background in electricity & magnetism physics.

Grading

- 30% Homework (9 problem sets)
- 20% Exam 1
- 20% Exam 2
- 30% Final

Homework

- Homework is due on Fridays at 5:00pm via upload on Courseworks. Your lowest score will be dropped. Late homework will be accepted within 48 hours with the following penalty: -20% for 0-24 hours late, and -40% for 24-48 hours late. No late homework will be accepted after this point.
- Seriously – don't email us to request homework extensions!
- If you experience issues uploading to Courseworks, you must email the homework to the TA and instructor by the deadline along with a screenshot of your CUIT ticket requesting help
- Collaboration between students on homework is allowed. Each student is responsible for turning in his or her own assignment in full.

Exams

- This course has two closed-note exams that will be administered during class time. Formula and constants sheet will be provided.
- Tues. September 30th
- Tues. October 28th

Final

- The final exam will be comprehensive and administered at the time and location specified by the registrar.
- Tentative time: Thurs. December 18th 4:10-7pm

Course Content and Schedule

Sept 2nd	Introduction
Sept 4th	Crystal properties of semiconductors (S&B Chapter 1)
Sept 9th, 11th, 16th	Energy bands and charge carriers in semiconductors (S&B Chapter 3)
Sept 18th, 23rd	Excess carriers in semiconductors (S&B Chapter 4)
Sep 25th, **Sep 30th**, Oct 2nd, 7th, 9th, 21st	Junctions, diodes, device fabrication (S&B Chapter 5) **Exam 1 (S&B Chapters 1, 3, and 4)**
Oct 14th, 16th	Optoelectronic devices (S&B Chapter 8)
Oct 23rd, **28th**, 30th, Nov 6th, 11th	Bipolar Junction Transistors (S&B Chapter 7; C. Hu Chapter 8) **Exam 2 (S&B Chapters 5 and 8)**
Nov 13th, 18th	Metal-oxide-semiconductor capacitors (S&B Chapter 6, C. Hu Chapter 5)
No 20th, 25th, 2nd	Metal-oxide-semiconductor field-effect transistors (S&B Chapter 6, C. Hu Chapter 6 & 7)
Dec 4th	Last day of class, Extra-credit opportunity/review for final
Dec 18th	Final Exam

Course Communication

- **Courseworks:** CourseWorks is the main hub for this class. It will serve as a repository for all course files including homework assignments and solutions, grades, lecture slides, and lecture recordings. Homework assignments will also be submitted here.

- **Ed Discussion:** We will be using Ed Discussion, which is integrated into Courseworks, as an online discussion and communication tool. Rather than emailing questions on the homework or technical concepts to the teaching staff , we encourage you to post your questions on Ed Discussion. Questions reach and benefit all students in the class. The staff will do our best to answer questions promptly.

Textbook

Required: B. G. Streetman, S. K. Banerjee, *Solid State Electronic Devices*, 7th ed., Pearson/Prentice Hall, 2014. ISBN-10: 0133356035. ISBN-13: 978-0133356038.

Required (free online): C. C. Hu, *Modern Semiconductor Devices for Integrated Circuits*, 3rd ed., Wiley, 2007. (https://www.chu.berkeley.edu/modern-semiconductor-devices-for-integrated-circuits-chenming-calvin-hu-2010/)

Other Recommended Resources

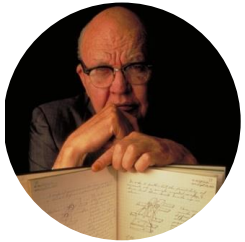
- B. Van Zeghbroeck , *Principles of Semiconductor Devices,* a free online textbook. (https://www.eletrica.ufpr.br/graduacao/e-books/Principles%20Of%20Semiconductor%20Devices.pdf)
- D. K. Bhattacharya, R. Sharma, *Solid State Electronic Devices*, 2nd edition, Oxford Univeristy Press, 2013. (available for free through Columbia libraries/Knovel. Click next to green checkmark here: https://clio.columbia.edu/catalog/12110723?counter=1)
- R. F. Pierret, *Semiconductor Device Fundamentals*, Addison-Wesley, 1996.
- ECE 440 on nanoHUB (https://nanohub.org/resources/5221)
- Britney Spears' guide to semiconductor physics (http://britneyspears.ac/lasers.htm)

The Semiconductor Revolution

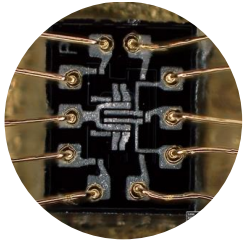

1947
Invention of the transistor
Shockley, Bardeen, Brattain
Bell Labs

Point-contact transistor

1956
Noble Prize in Physics awarded for the discovery of the transistor
Shockley, Bardeen, Brattain
Bell Labs



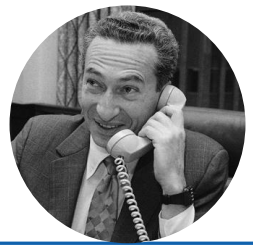

1958
Invention of the integrated circuit
Jack Kilby
Texas Instruments

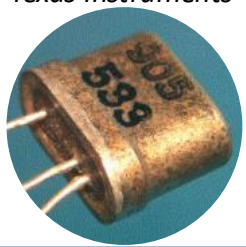
1961
Logical NOR gate integrated circuit used on Apollo mission.
Fairchild Semiconductor, Raytheon, Philco Ford

1954

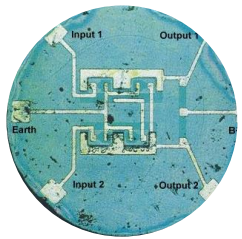
Invention of the silicon transistor
Morris Tanenbaum
Bell Labs



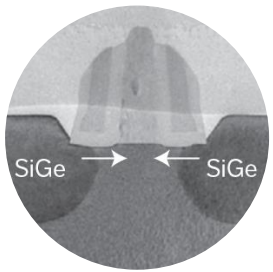
First commercially available silicon transistor
Gordon Teal
Texas Instruments



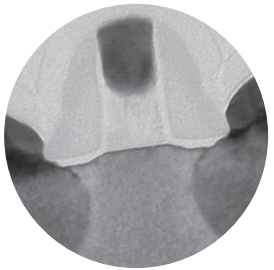
1959
First patent awarded for the monolithic integrated circuit
Robert Noyce
Fairchild Semiconductor

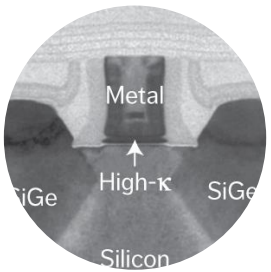
The Cycle of Innovation



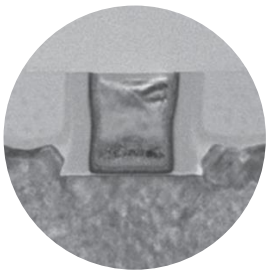
2003
90 nm



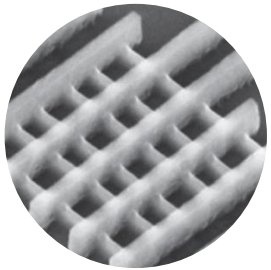
2005
65 nm



2007
45 nm



2009
32 nm



2011
22 nm

2014
14 nm

Transistor Scaling

Investment

Better Performance/Cost

Market Growth

1944
Mainframe

1965
Mini-Computer

1973
Workstation

1977
Personal Computer

1988
Laptop

2007
Smartphone

Moore's Law

"Transistor density on integrated circuits doubles about every two years"

1965

Gordon Moore

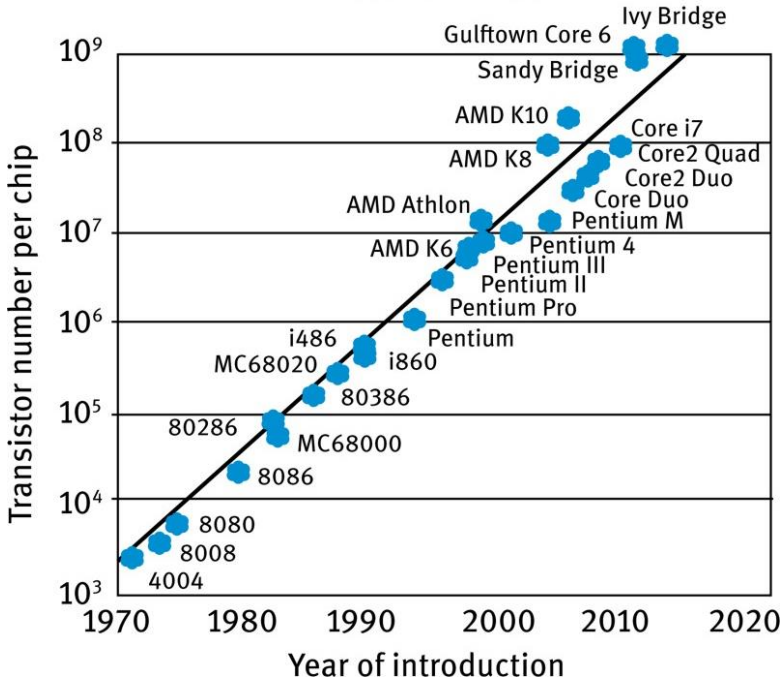


Image Credits: Wired, © 2015 A. Ostendorf and K. König, published by De Gruyter.

The Traitorous Eight

- Group of 8 employees who left Shockley Semiconductor Laboratory in 1957
- Formed Fairchild Semiconductor
- Became incubator for silicon valley
- “Fairchildren” companies include…
  - Intel
  - AMD
  - Intersil
  - National Semiconductor

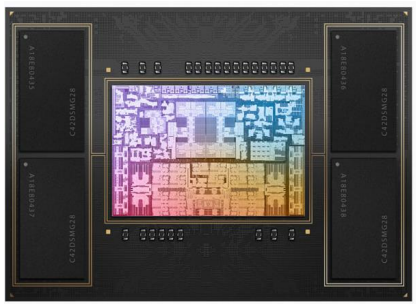
From left to right: Gordon Moore, C. Sheldon Roberts, Eugene Kleiner, Robert Noyce, Victor Grinich, Julius Blank, Jean Hoerni and Jay Last (1960)

Image Credits: Wikipedia

The Billions of Semiconductor Devices We Carry on Us

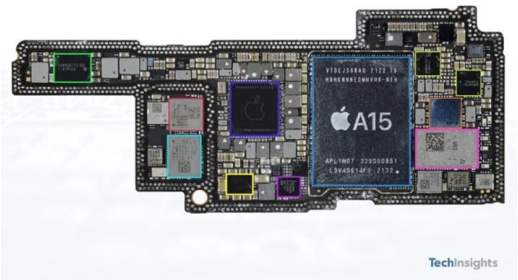
Macbook Air

20 billion Si transistors
Apple M2 chip
5 nm fabrication



iPhone 14

15.8 billion Si transistors
Apple A15 Bionic chip
5 nm fabrication processes



Don't forget about MEMS and sensors!

Micro electro-mechanical system (MEM

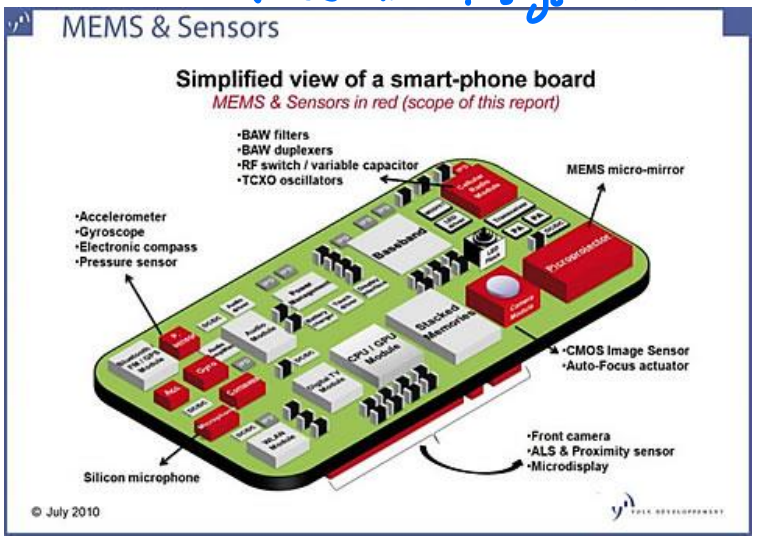


Image Credits: Apple, TechNave, Engineering.com

What does “solid state” mean?

Devices use semiconductor materials (solid state of matter) to manipulate electricity

As opposed to…? Vacuum tubes → use gas to transport electrons

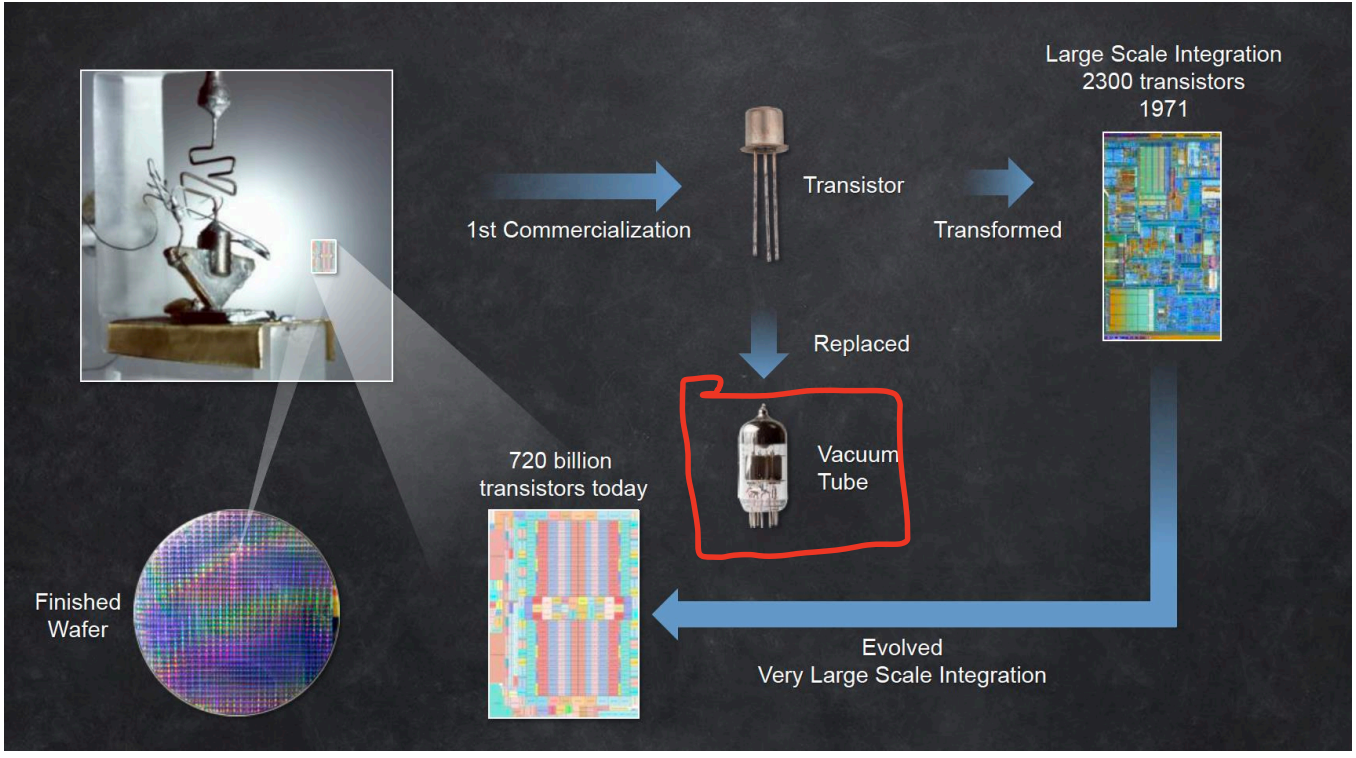


Image Credits: Dr. Thomas Caulfied

The Semiconductor Industry

Chemical Engineering

Chemistry

Materials Science

Nuclear Physics

Electrical Engineering

Mechanical Engineering

Applied Physics

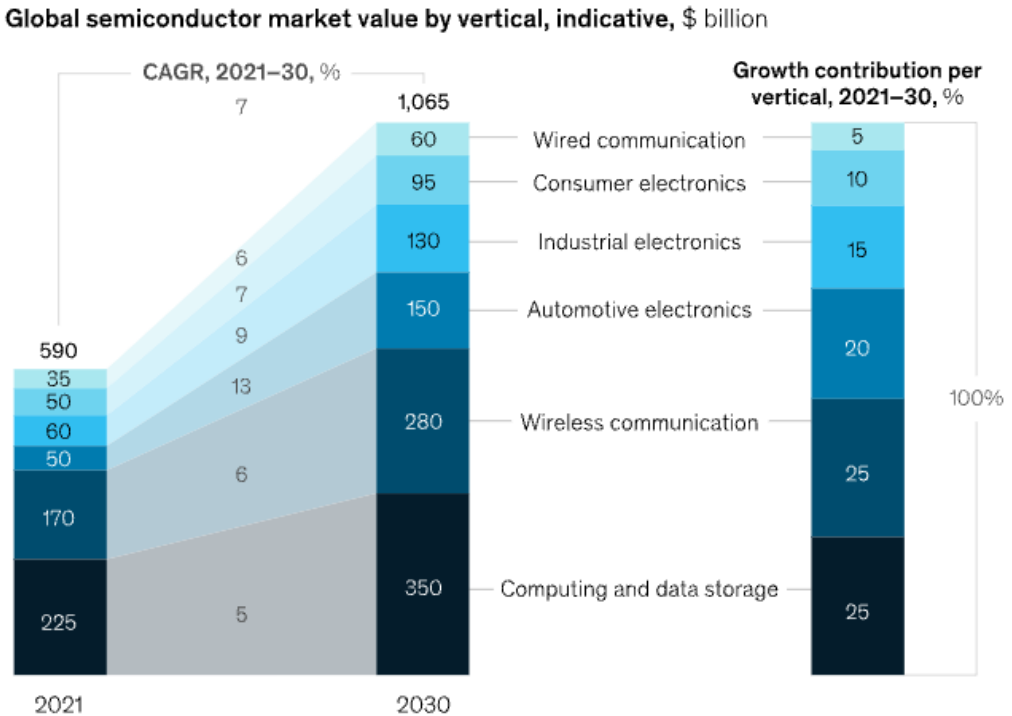
Muti-Disciplinary!

Slide Credit: Prof. Roger Howe

The Semiconductor Industry

Global Market: $600 billion (2021)

Market Predictions: $1 trillion (2030)



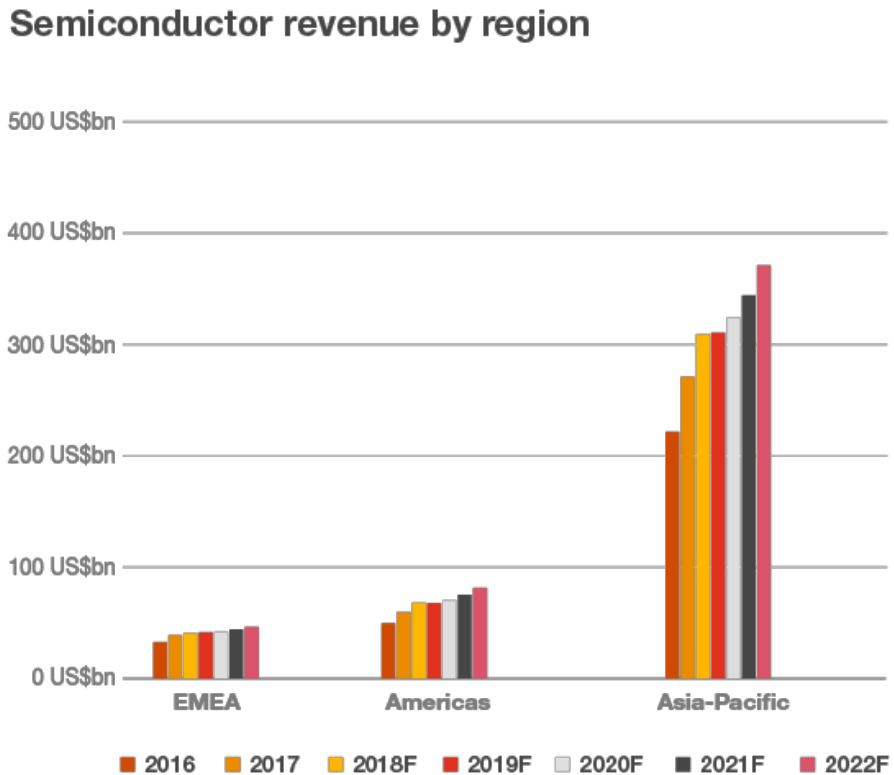
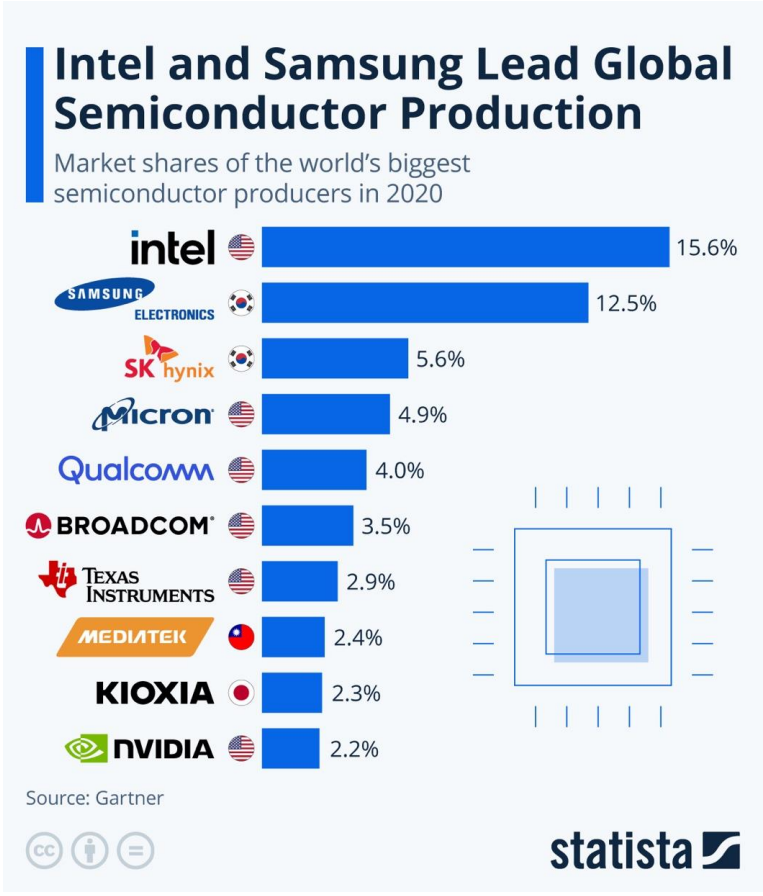


Image Credits: McKinsey & Company, PwC Research

Key Players in the Industry



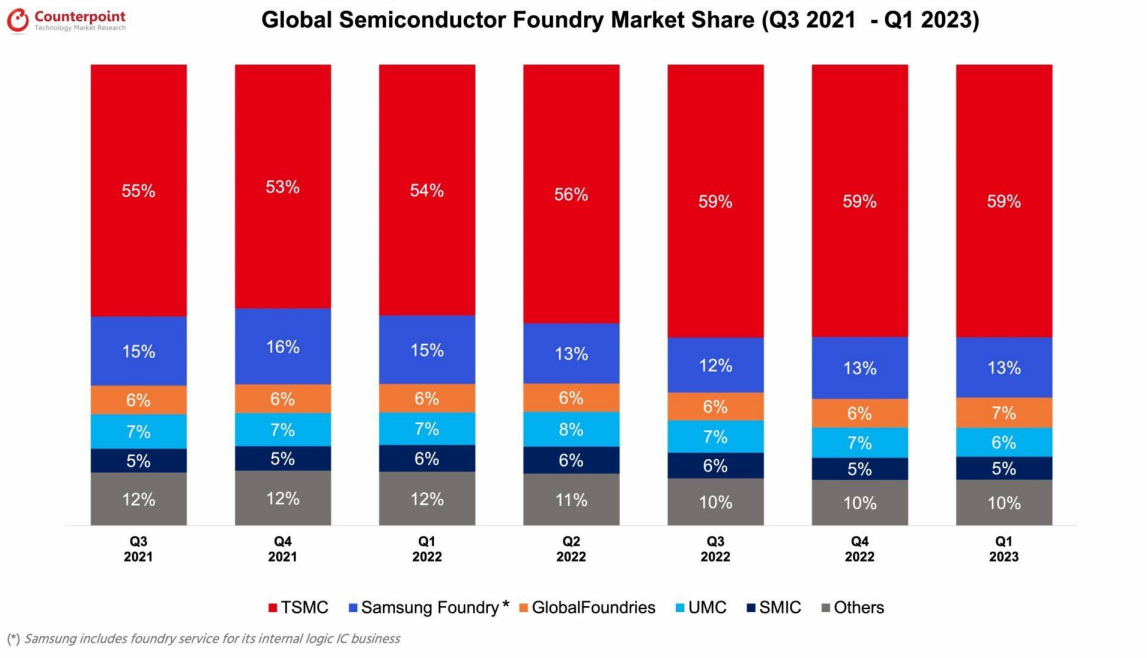


Image Credits: Statista, Counterpoint

The Semiconductor Industry Ecosystem

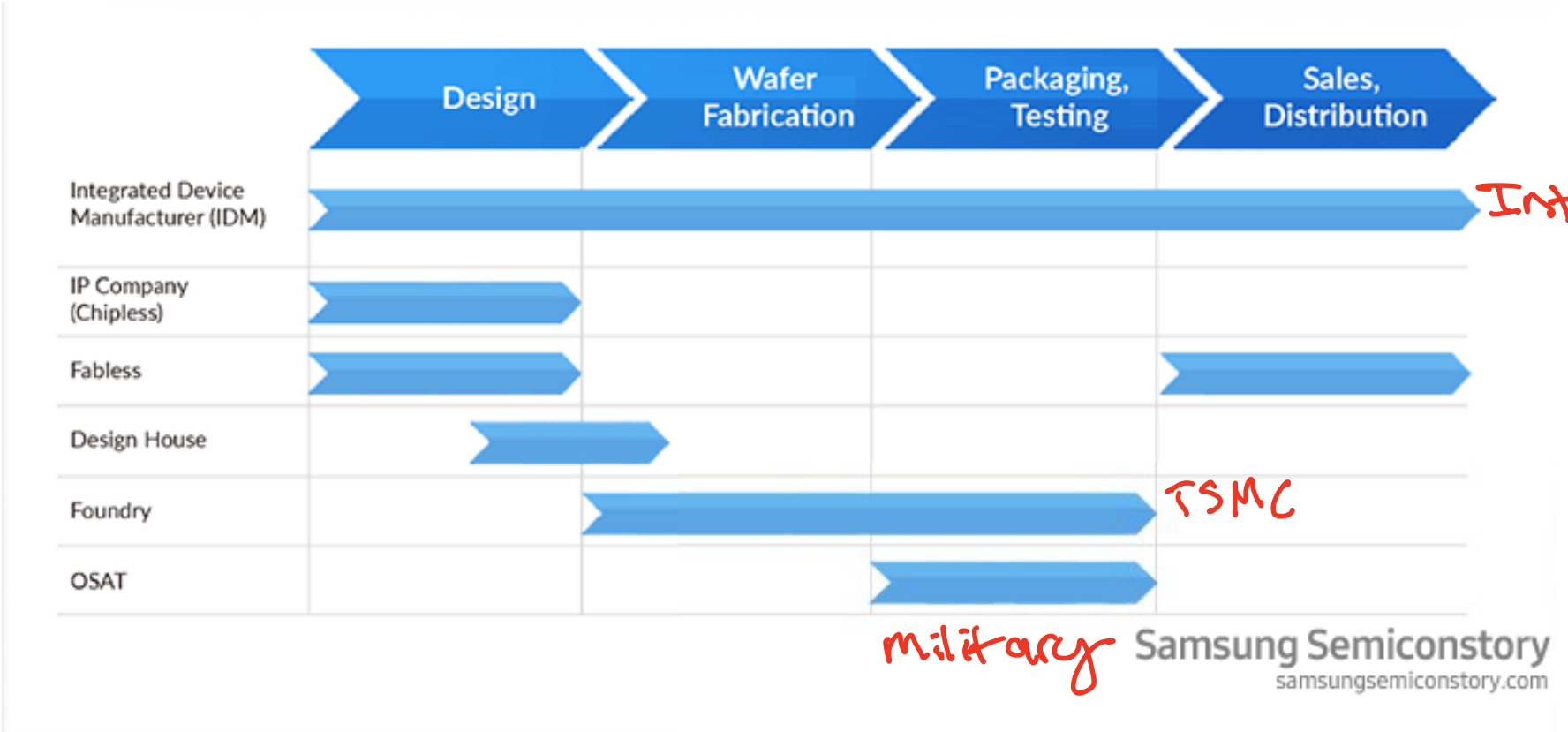


Image Credits: Samsung Semiconstory

Recent Chip Shortage

- Strong demand and no supply
- Highlighted how critical chips are to the global economy!
- Countless products canceled, halted, delayed, or prices skyrocketed

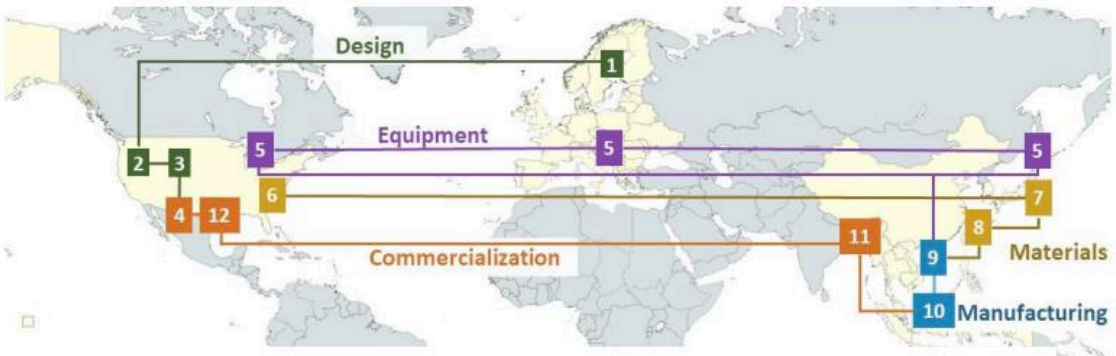


Figure 3: A Simplified Outlook on the Global SSC inspired from (Varas et al., 2021).

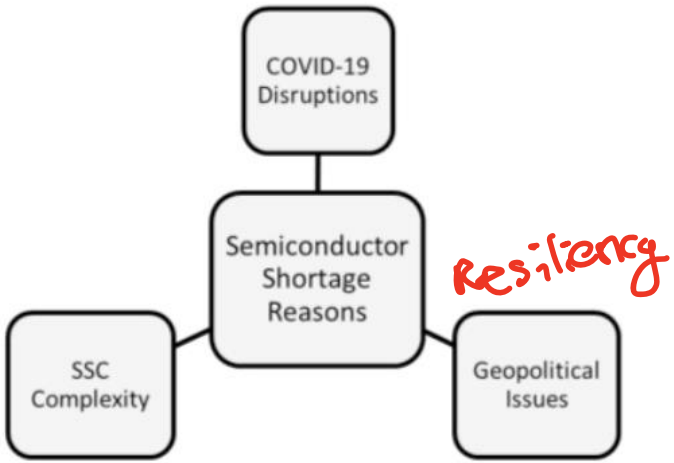
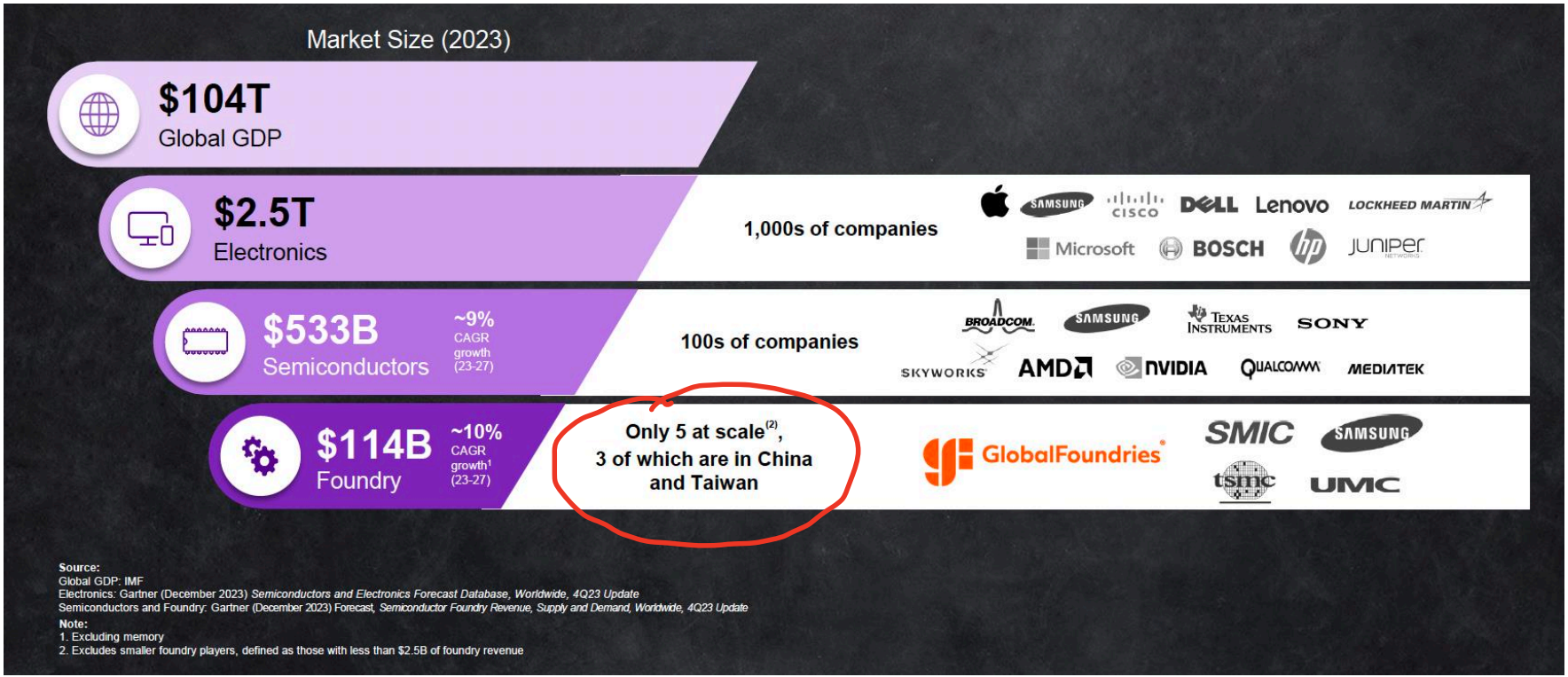


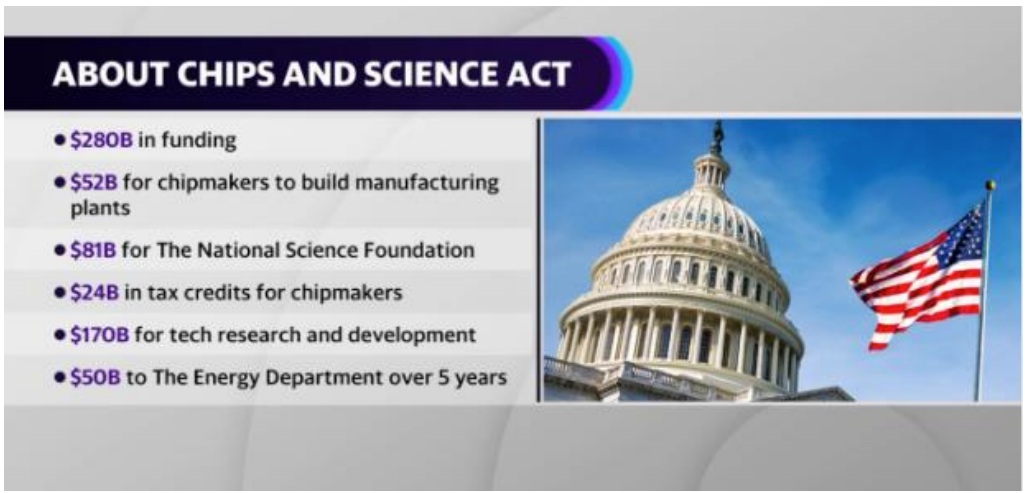
Image Credits: doi: 10.1016/j.ifacol.2022.09.439

Concentration of Manufacturing: Industrial and Geographical



The CHIPS Act and Workforce Development

- Funding to boost domestic research and manufacturing
- Signed in 2022
- Help to develop skilled STEM workforce



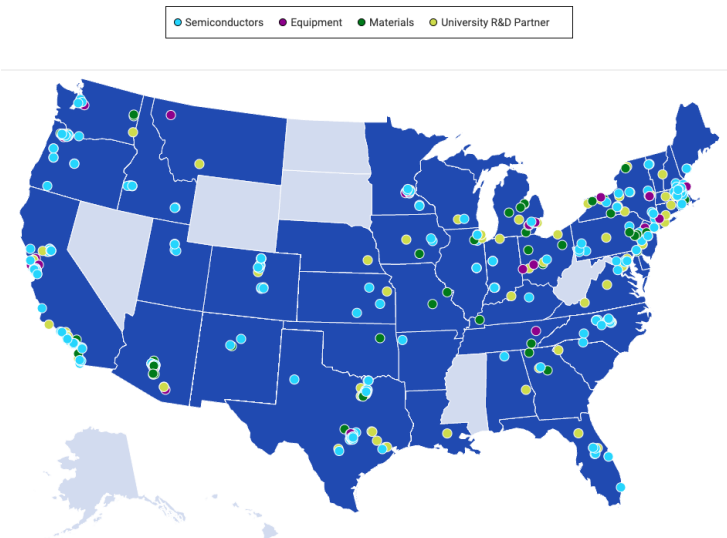


Image Credits: Yahoo, Washington Post, Semiconductor Industry Association

Future Trends Driving the Semiconductor Industry

Artificial intelligence

Internet of Things (IoT)

Autonomous vehicles

5G and AR/VR

Image Credits: Forbes, MIT News, IEEE Innovation at Work, XR Today

The Impact of Moore's Law

"Transistor density on integrated circuits doubles about every two years"

The Good: Shrinking Consumer Electronics

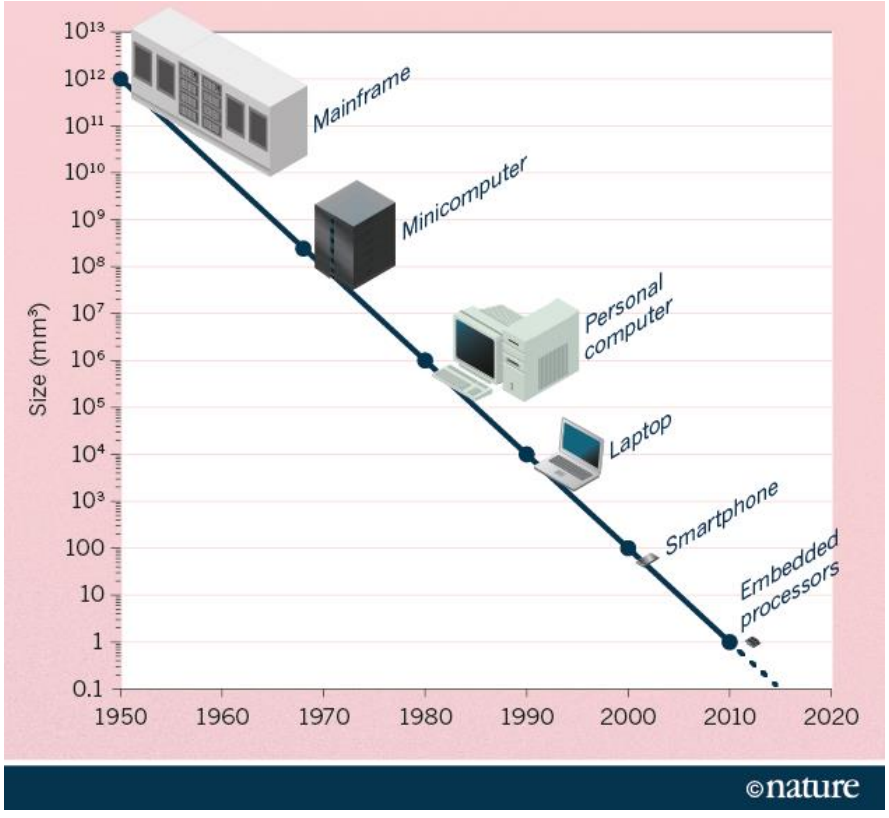


Image Credits: The Chips are Down for Moore's Law, *Nature* (Feb. 2016)

The Impact of Moore's Law

"Transistor density on integrated circuits doubles about every two years"

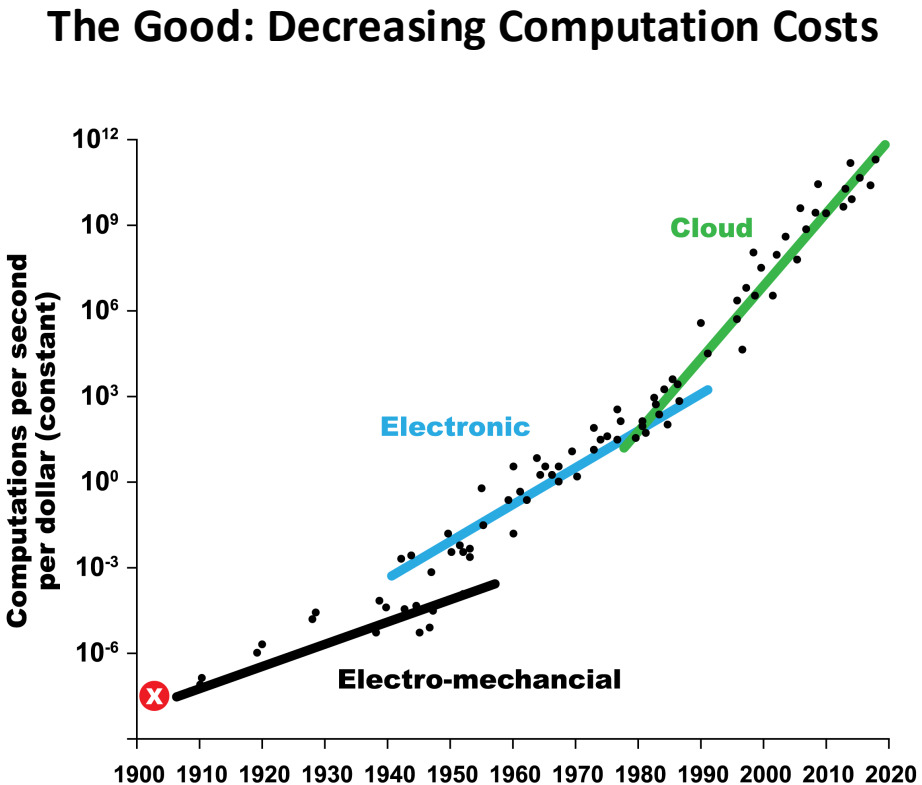


Image Credits: AEI.org

The Impact of Moore's Law

What if the automotive industry had achieved the incredible pace of innovation as the semiconductor industry?

A Rolls Royce would cost only $40

and

could circle the globe 8 times on **1 gallon of gas**

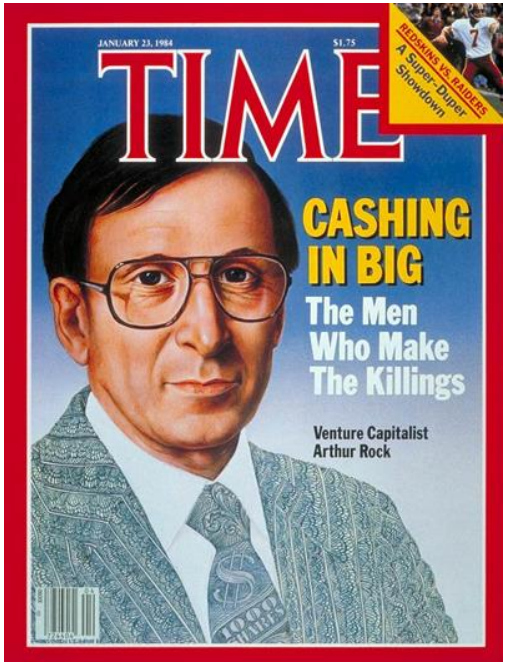
Source: McKinsey report on semiconductor industry

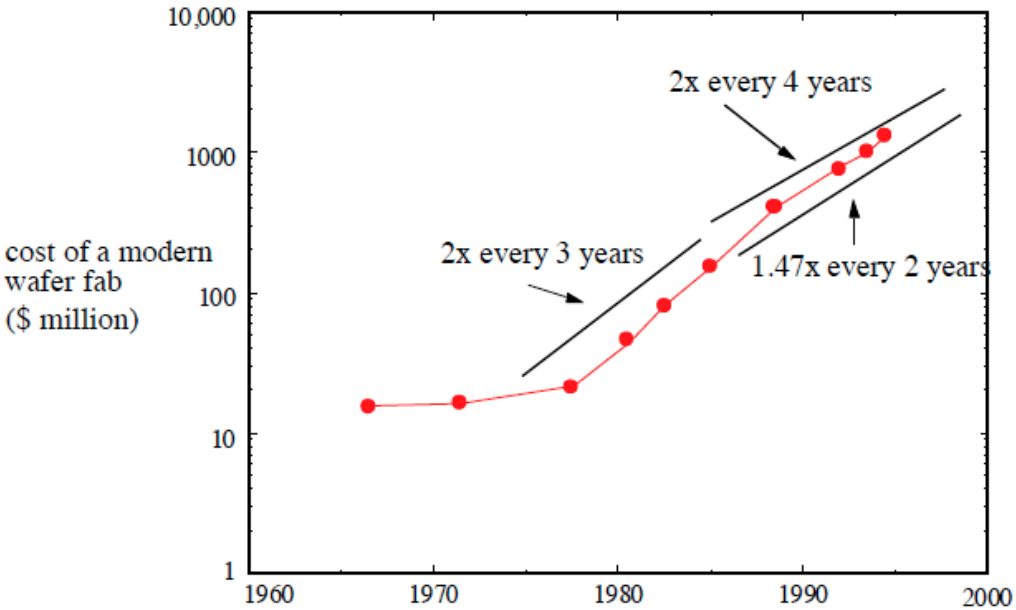
Image Credits: Dr. Thomas Caulfied

The Impact of Moore's Law: Rock's Law

"Cost of a semiconductor chip fabrication plant doubles every four years" – Arthur Rock

The Bad: As chips become more sophisticated, the cost increases





Today, to build a modern fab facility costs upwards of $10 billion. Only a few companies can afford this investment, leading to consolidation in the industry.

Image Credits: TIME, Roger Howe

International Technology Roadmap for Semiconductor (ITRS)

- To coordinate the market-driven cycle of Moore's law, the industry devised it's first roadmap in 1991
- Published by a consortium of international semiconductor experts
- Based on CMOS-only technology
- Represent the best opinion on the directions of research and 15 year projections

Year of Production	1998	2000	2002	2004	2007	2010	2013	2016	2018
Technology Node (half pitch)	250 nm	180 nm	130 nm	90 nm	65 nm	45 nm	32 nm	22 nm	14 nm
MPU Printed Gate Length		100 nm	70 nm	53 nm	35 nm	25 nm	18 nm	13 nm	10 nm
DRAM Bits/Chip (Sampling)	256M	512M	1G	4G	16G	32G	64G	128G	128G
MPU Transistors/Chip ($x10^b$)				550	1100	2200	4400	8800	14,000
Min Supply Voltage (volts)	1.8-2.5	1.5-1.8	1.2-1.5	0.9-1.2	0.8-1.1	0.7-1-0	06-0.9	0.5-0.8	0.5-0.7

ITRS - 2003 version

Image Credits: ITRS 2003 version, Roger Howe

International Technology Roadmap for Semiconductor (ITRS)

- "Transistors won't shrink beyond 2021"
- In reality, "roadmap" implies the future is well defined
- Huge technical challenges exist to actually achieving the forecasts of the roadmap

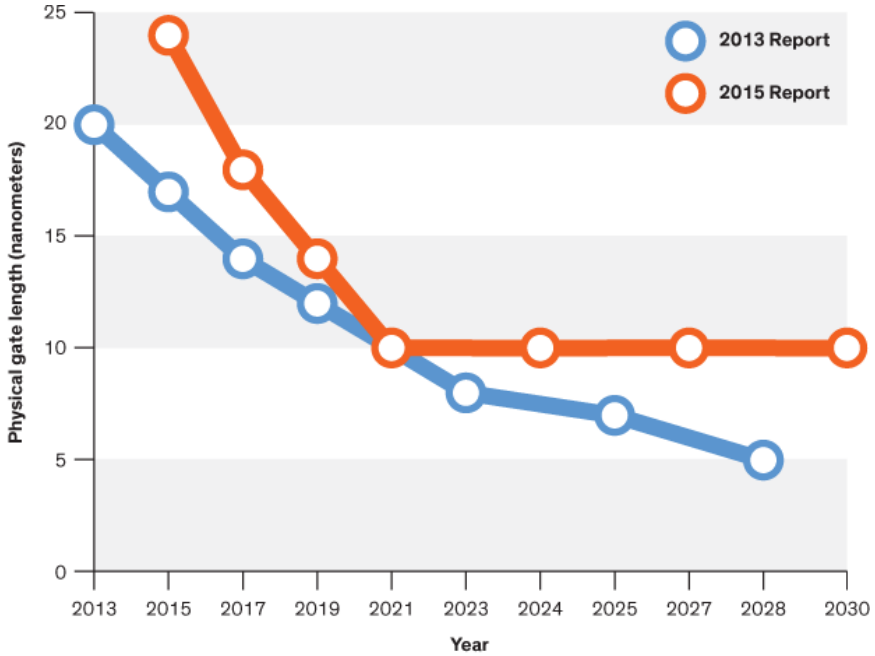
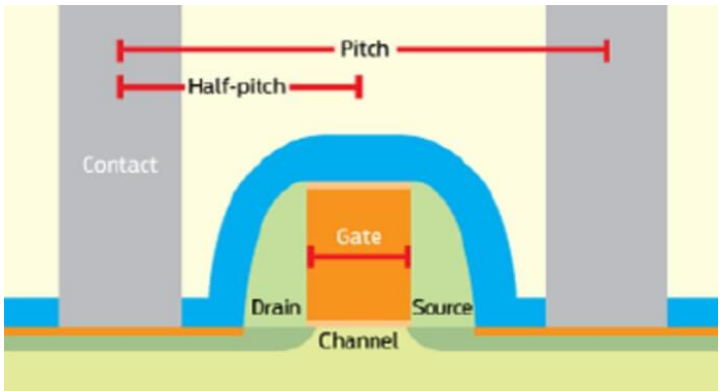


Image Credits: IEEE Spectrum

What is a technology node anyways?

- Smaller the node = smaller the feature size
- Historically, the node referred to # of features like gate length and the half-pitch
- But, discrepancies among foundries means the node has lost some of its meaning

Intel "22 nm" node transistors have
$L_G \approx 35$ nm, $t_{fin} \approx 8$ nm, pitch ≈ 90 nm



Year	Node	Half-Pitch	Gate Length
2009	32	52	29
2007	45	68	38
2005	65	90	32
2004	90	90	37
2003	100	100	45
2001	130	150	65
1999	180	230	140
1997	250	250	200
1995	350	350	350

Qualcomm "28 nm" node Snapdragon

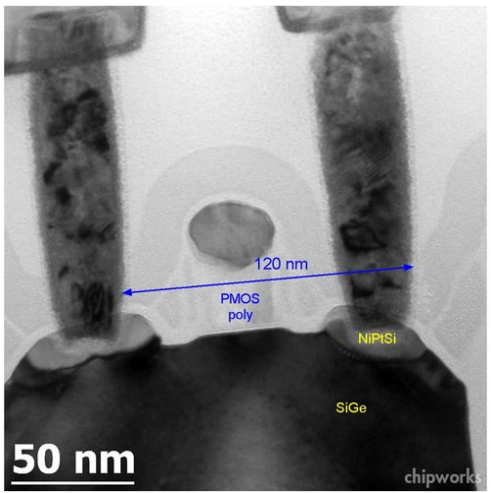
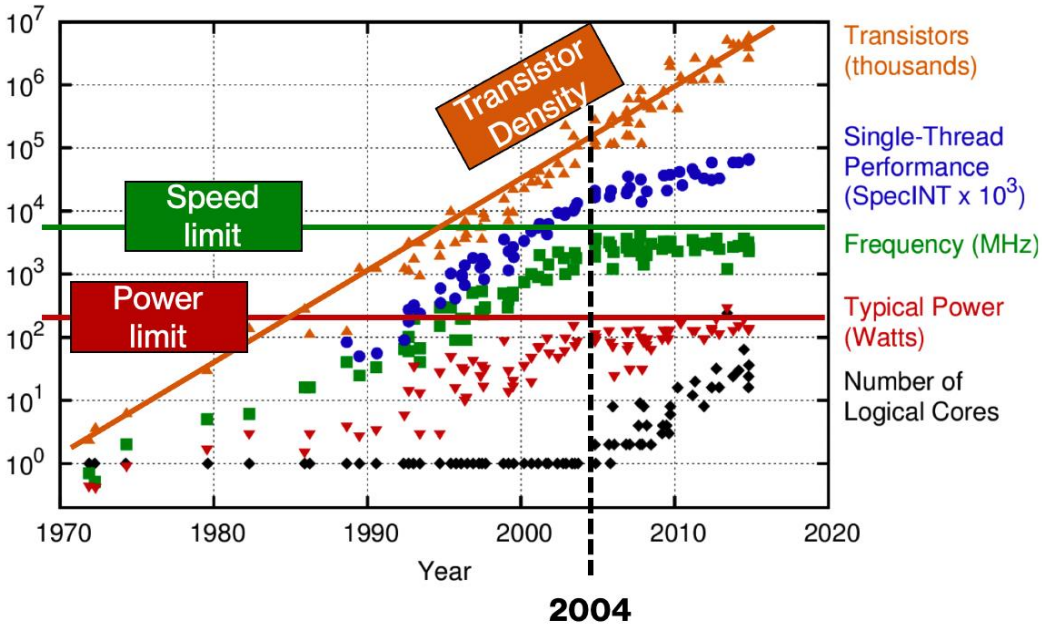
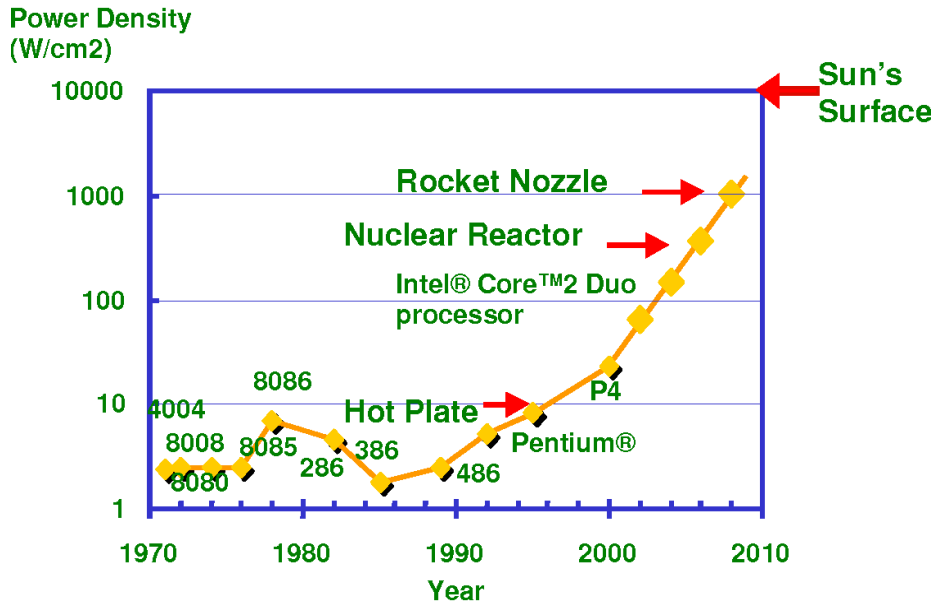


Image Credits: 3dincites, AnySilicon Semipedia, TechInsights

The End of Moore's Law?

Moore's Law holds in density, but performance plateaus





At the same time, demand is higher than ever!

Image Credits: Dell Education Services, arxiv: https://arxiv.org/pdf/1406.3790.pdf

What Comes Next

- Scaling alone is not enough
- Immense challenges (and opportunities!) for the industry

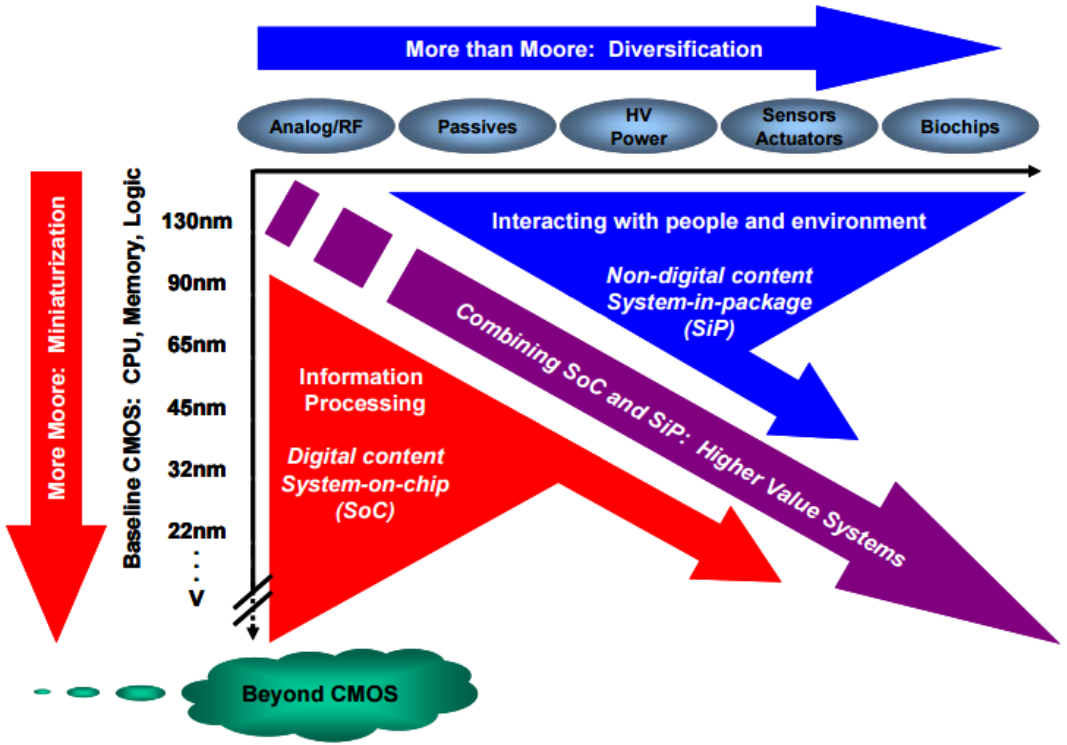


Image Credits: HAL Id: tel-00952978

More Moore Challenges: Miniaturization

- Collision of money limitations and physics limitations
- Quantum effects begin to dominate!

- EUV lithography necessary for Angstrom era
- Price: $75m+, and you need 15 for a large fab

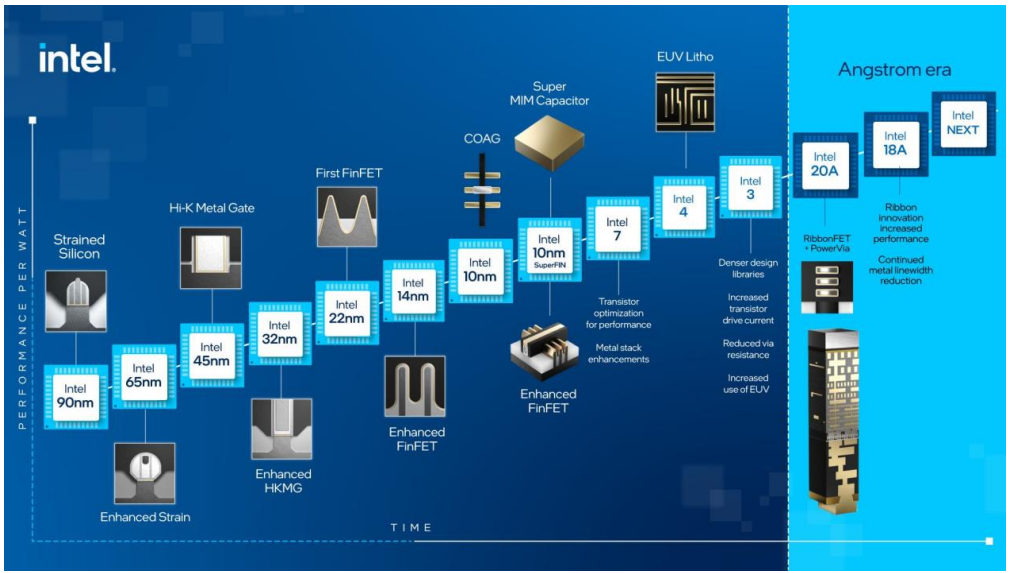


Image Credits: Intel, Laser Focus World

More Moore: Device Innovations and "Beyond CMOS"

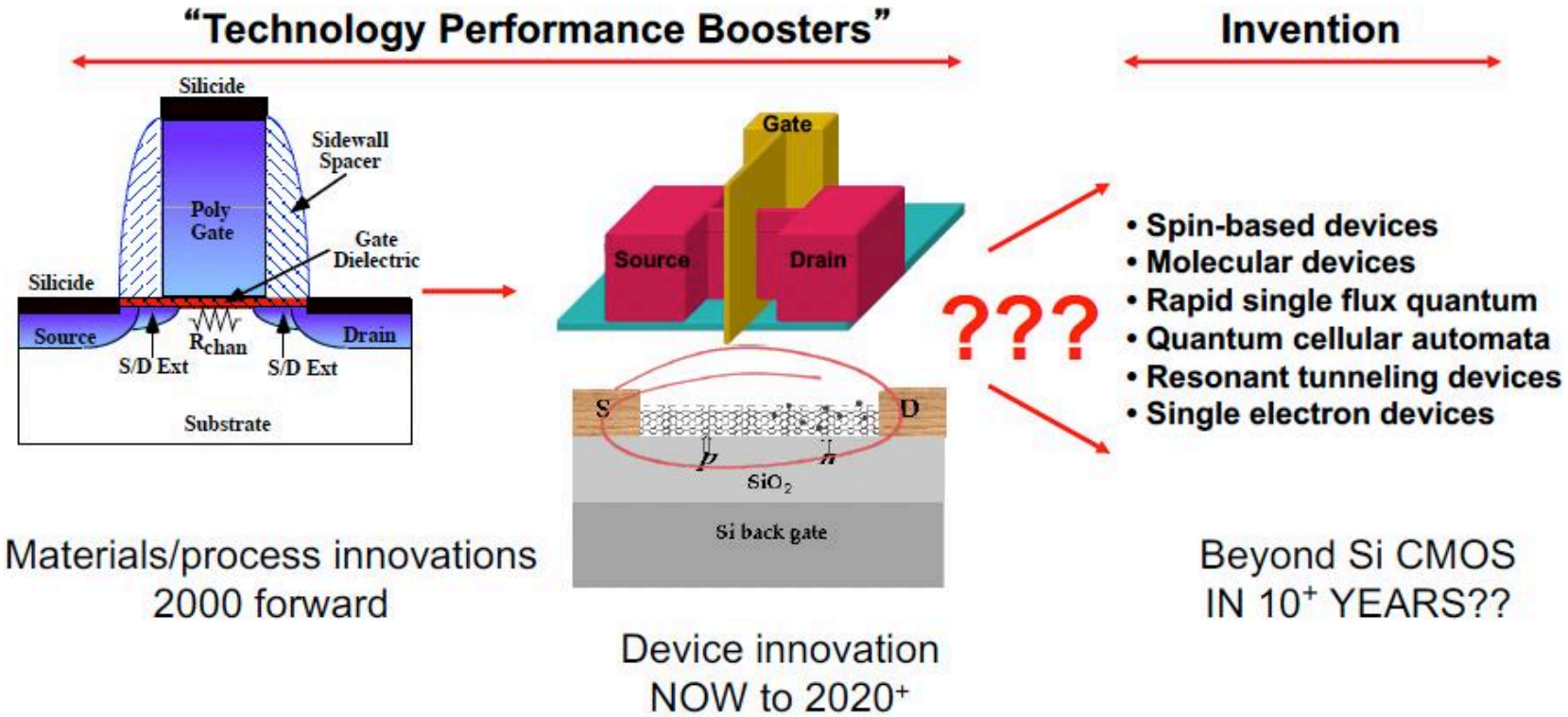


Image Credits: Roger Howe, Stanford EE 216 Course

Why Silicon?

- Easily purified and grown as a single crystal
- Reasonably good electrical properties
- Si and SiO_2 are highly manufacturable (ease of fabrication)
- Si has great mechanical properties (not fragile)
- Si is abundant in nature
- Easily passivated by SiO_2 (a great insulator w/ high etch selectivity to Si)

But Si is limited

- Indirect bandgap --> not good for optoelectronics
- Only moderate carrier mobility

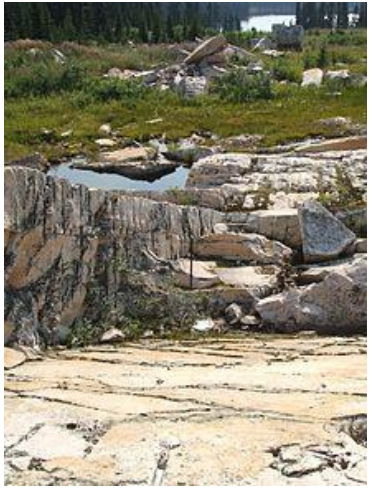
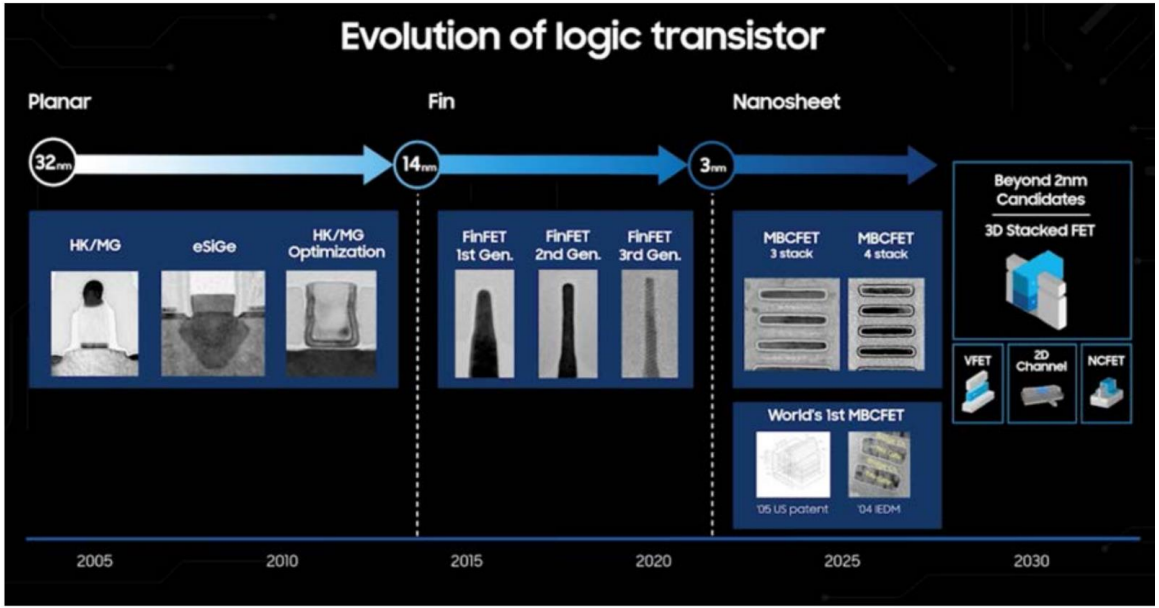


Image Credits: AnySilicon, Wikipedia

More Moore: 3D topology



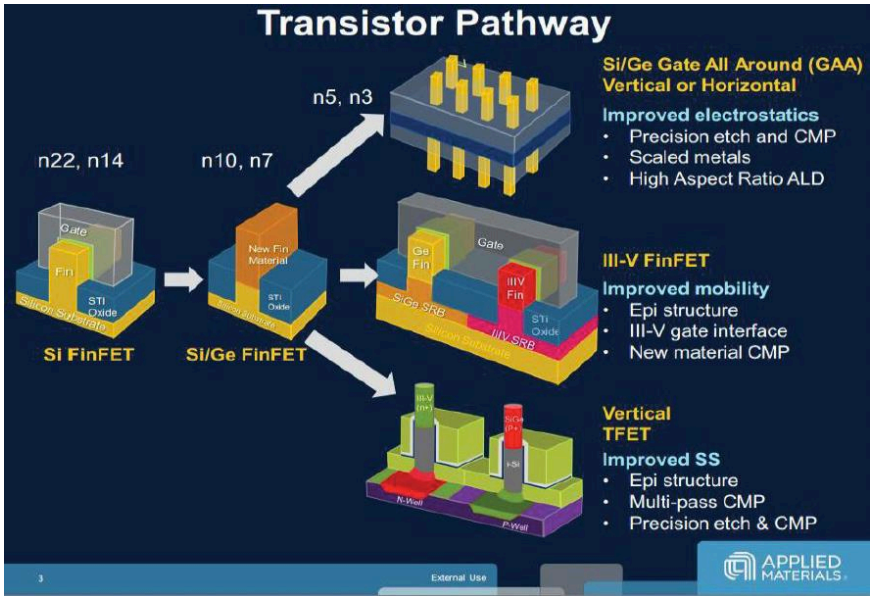
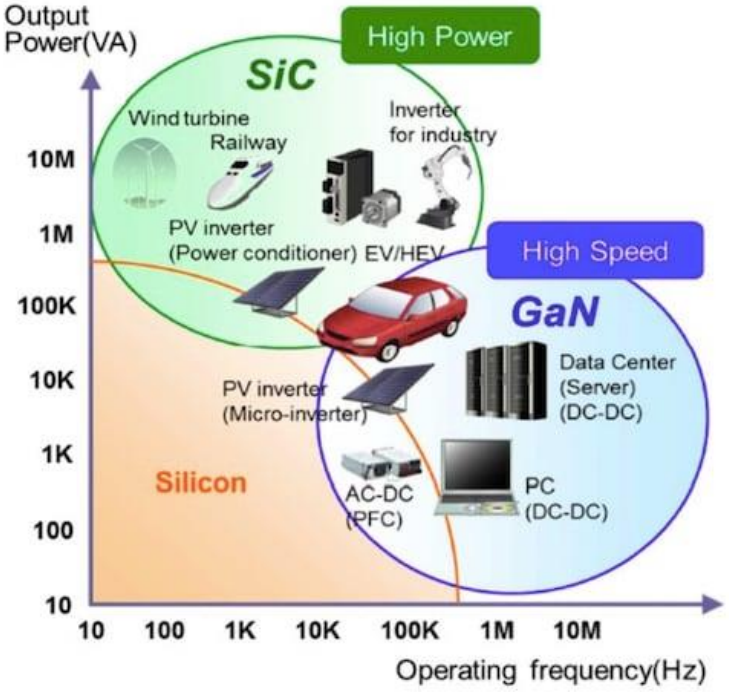


Image Credits: IRDS 2022 Report, Applied Materials

More than Moore: Material Innovations "Beyond Silicon"

- (Ultra)wide bandgap semiconductors AKA (U)WBG for high power, high frequency, harsh environment applications, optoelectronics



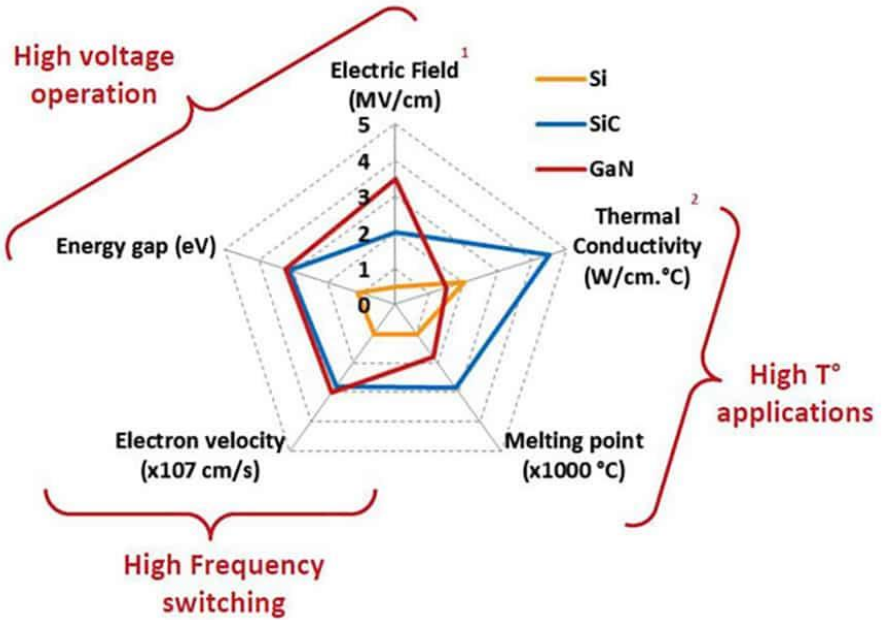
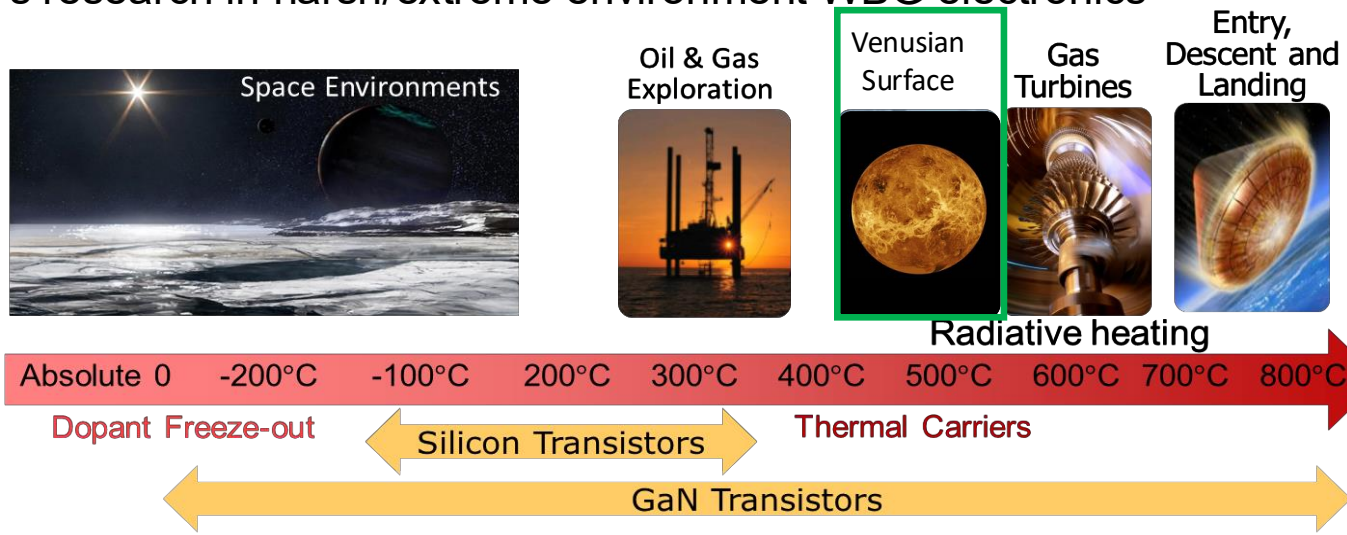
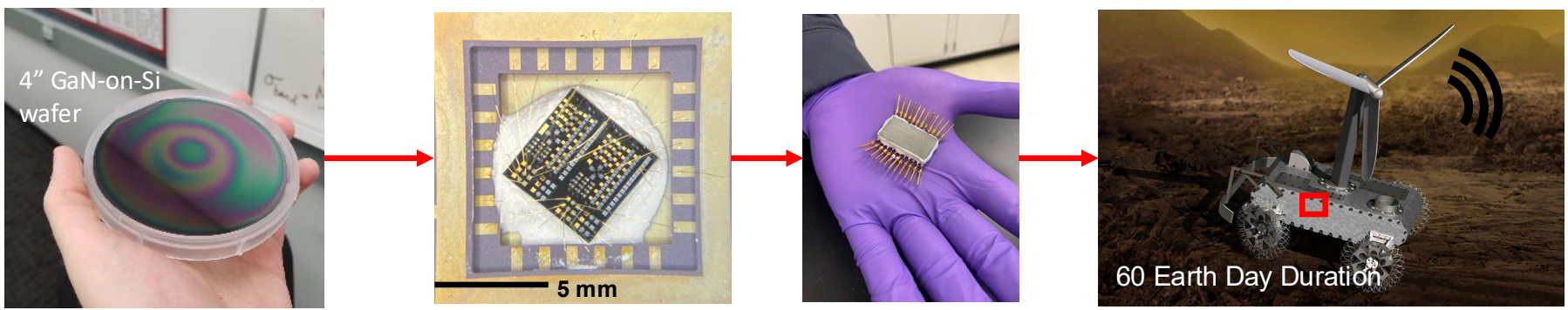


Image Credits: doi:10.1088/1757-899X/738/1/012004, Navitas Semiconductor

More than Moore: Material Innovations "Beyond Silicon"

- Prof. Eisner's research in harsh/extreme environment WBG electronics

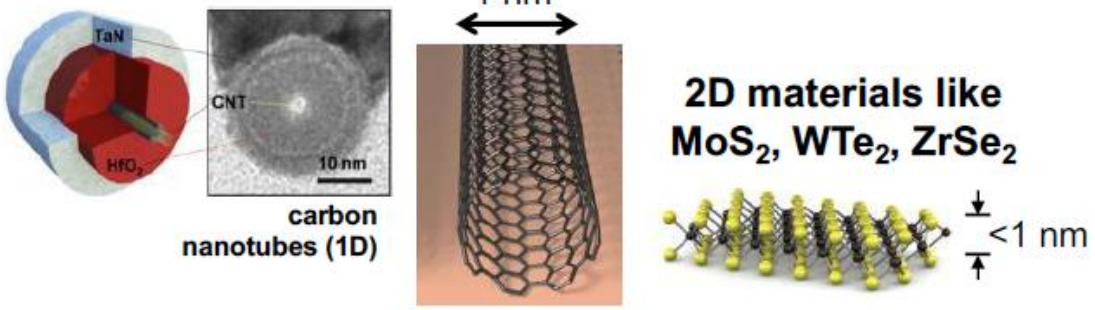




Envisioned GaN chip providing sensing + telecommunication on Venus rover

More than Moore: Material Innovations "Beyond Silicon"

- Current transistors carved out of bulk 3D materials like Si using patterning, etching, etc
- As 3D materials shrink, they have dangling bonds and surface states
- These effects, and quantum mechanics, likely limit minimum dimensions to a few nm
- Will 21st century transistors be made of 1D (carbon nanotube) or 2D (graphene, MoS_2) materials?



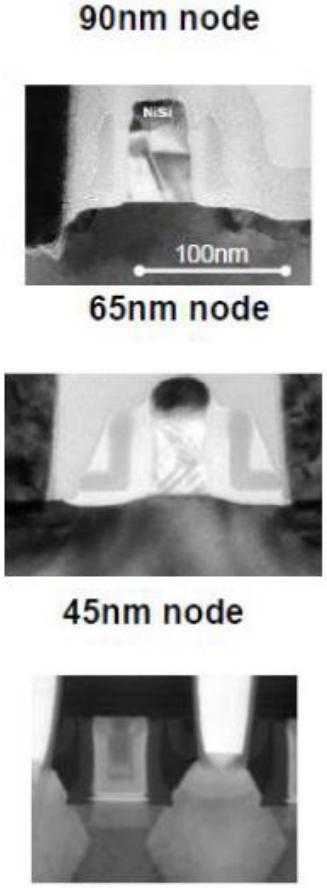
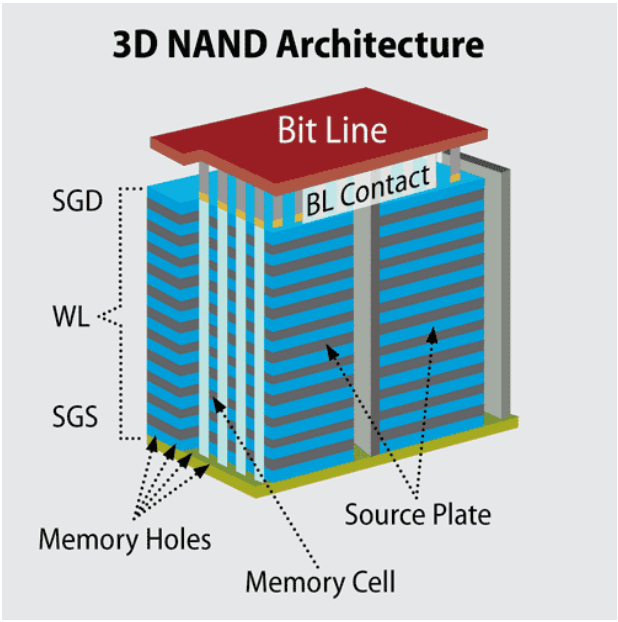


Image Credits: Roger Howe, Stanford EE 216 Course

More than Moore: 3D Integration

- “Skyscrapers”
- Already in use in memory architectures
- Can be deposited layer by layer with flexible printed electronics and 1D/2D



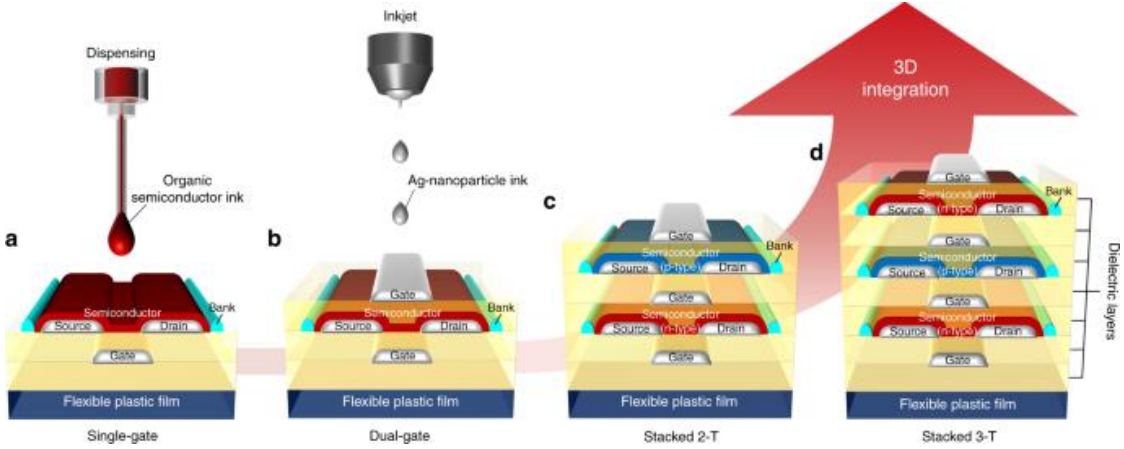
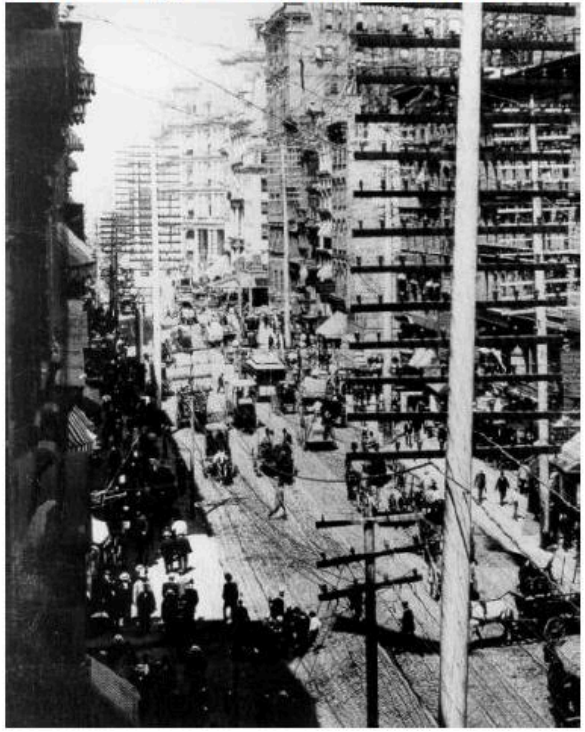


Image Credits: Enterprise Storage Forum, doi: 10.1038/s41467-018-07904-5

More than Moore: 3D Integration

Communications Challenge

Broadway, New York City, 1887



Intel Microprocessor, 2005

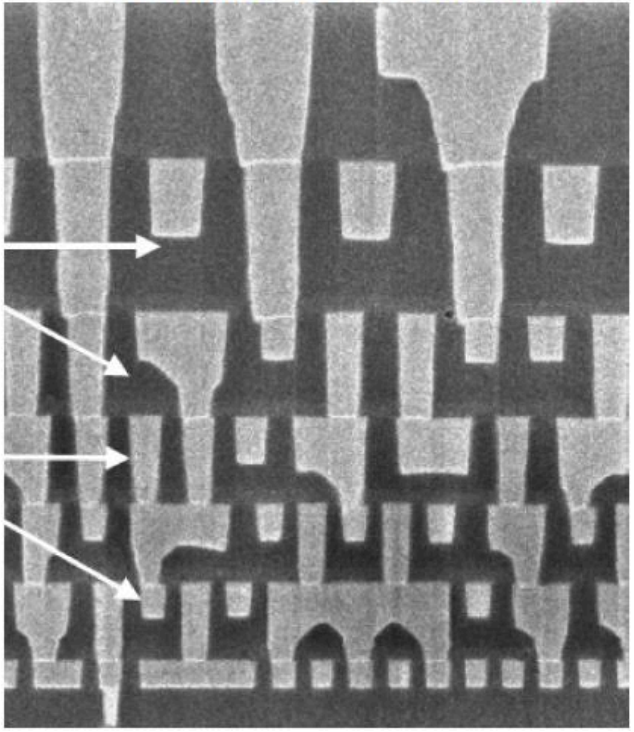
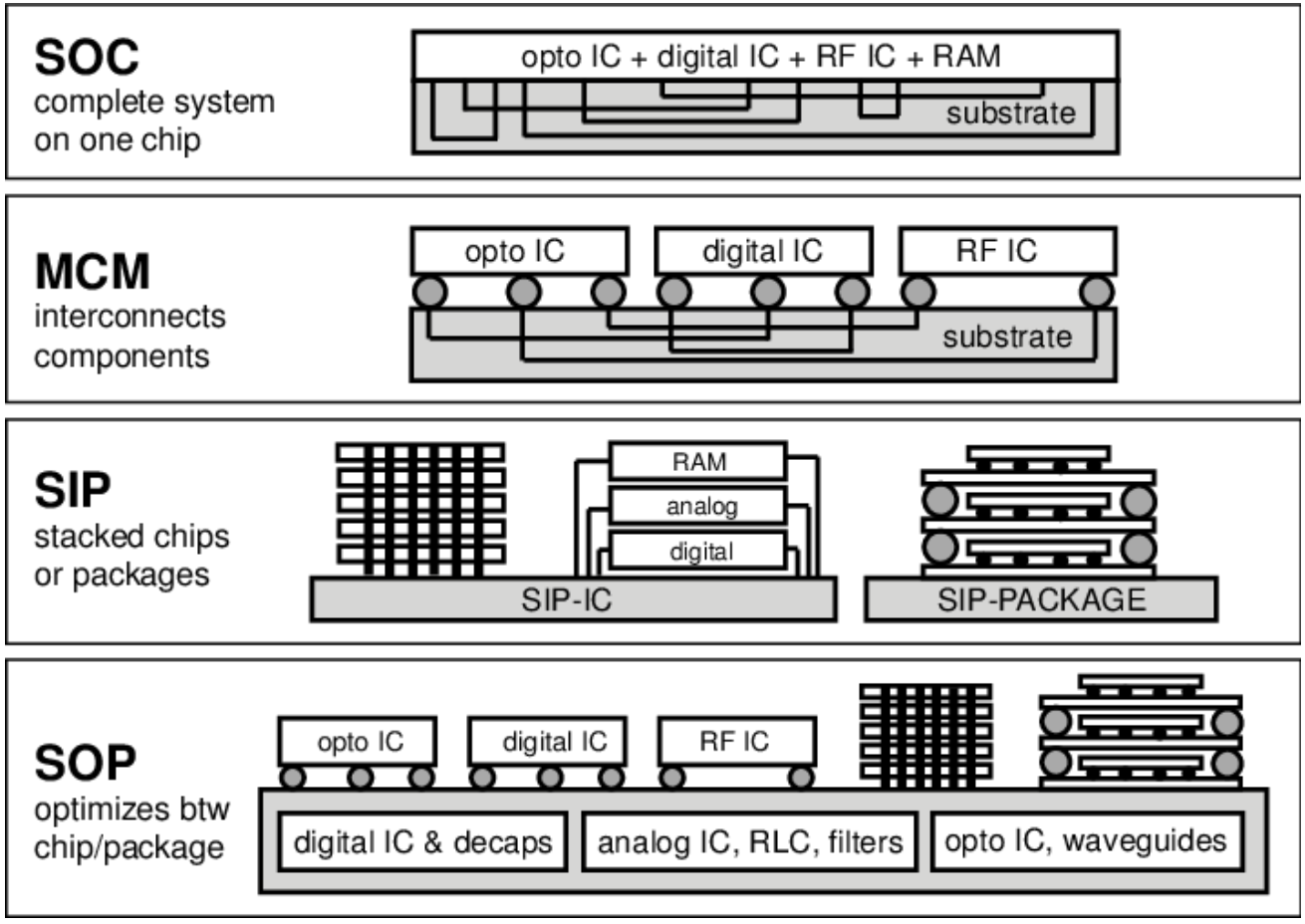


Image Credits: Roger Howe, Stanford EE 216 Course

More than Moore: Advanced Packaging



•Image Credits: DOI: 10.1109/ECTC.2005.1441368

More than Moore: Heterogeneous Integration

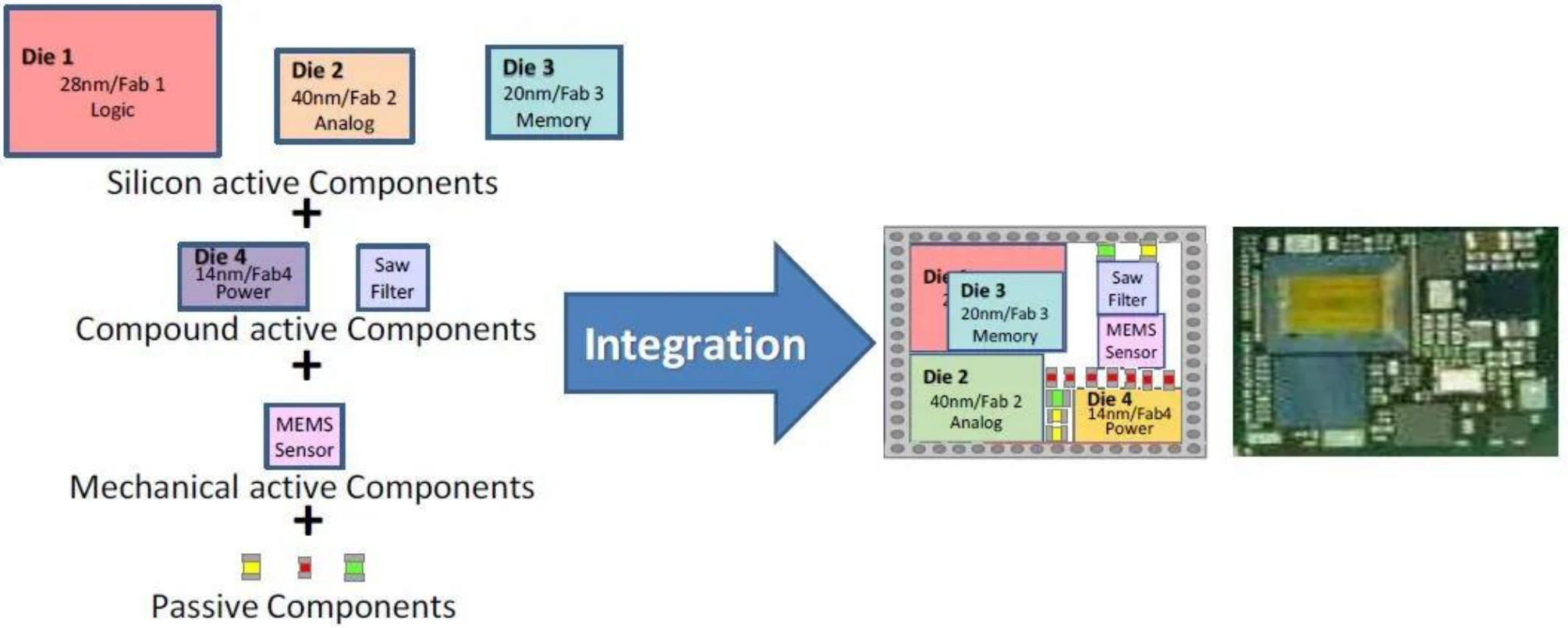
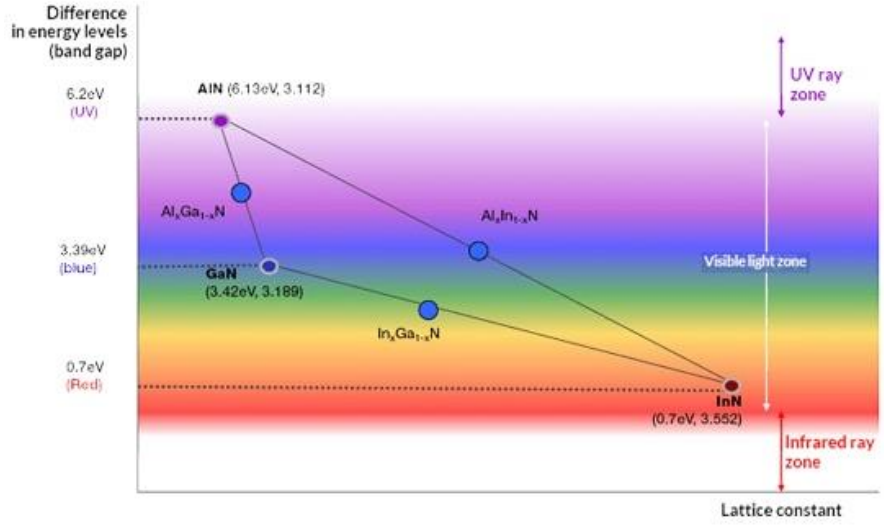


Image Credits: EDN

More than Moore: Integration of Electronics and Photonics

- Driven by requirements for smart optical networks, greater bandwidths and lower costs
- Interconnect bottleneck for CMOS operating above 10 GHz is pushing for integrated photonics for timing and possibly optical transmission
- Tremendous challenge: material incompatibility
  - Photonics require a different material for each wavelength
- Solutions: Hybrid integration, Si photonics



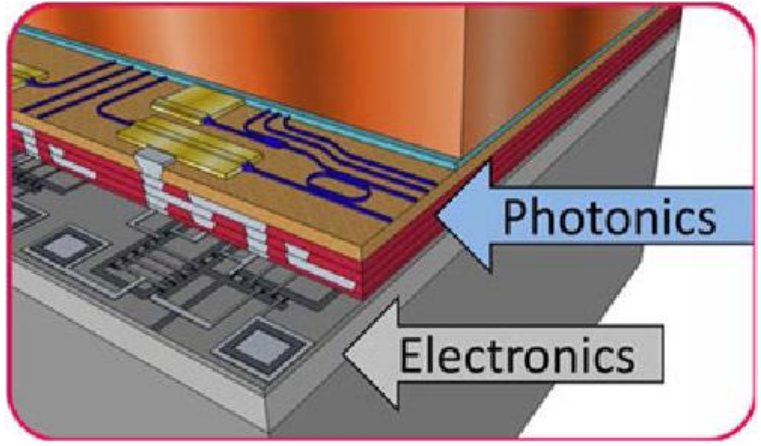


Image Credits: DOI:10.1109/JSTQE.2017.2772786, Samsung

MEMS devices

- Enabling sensors and actuators, new wearables, and so much more…

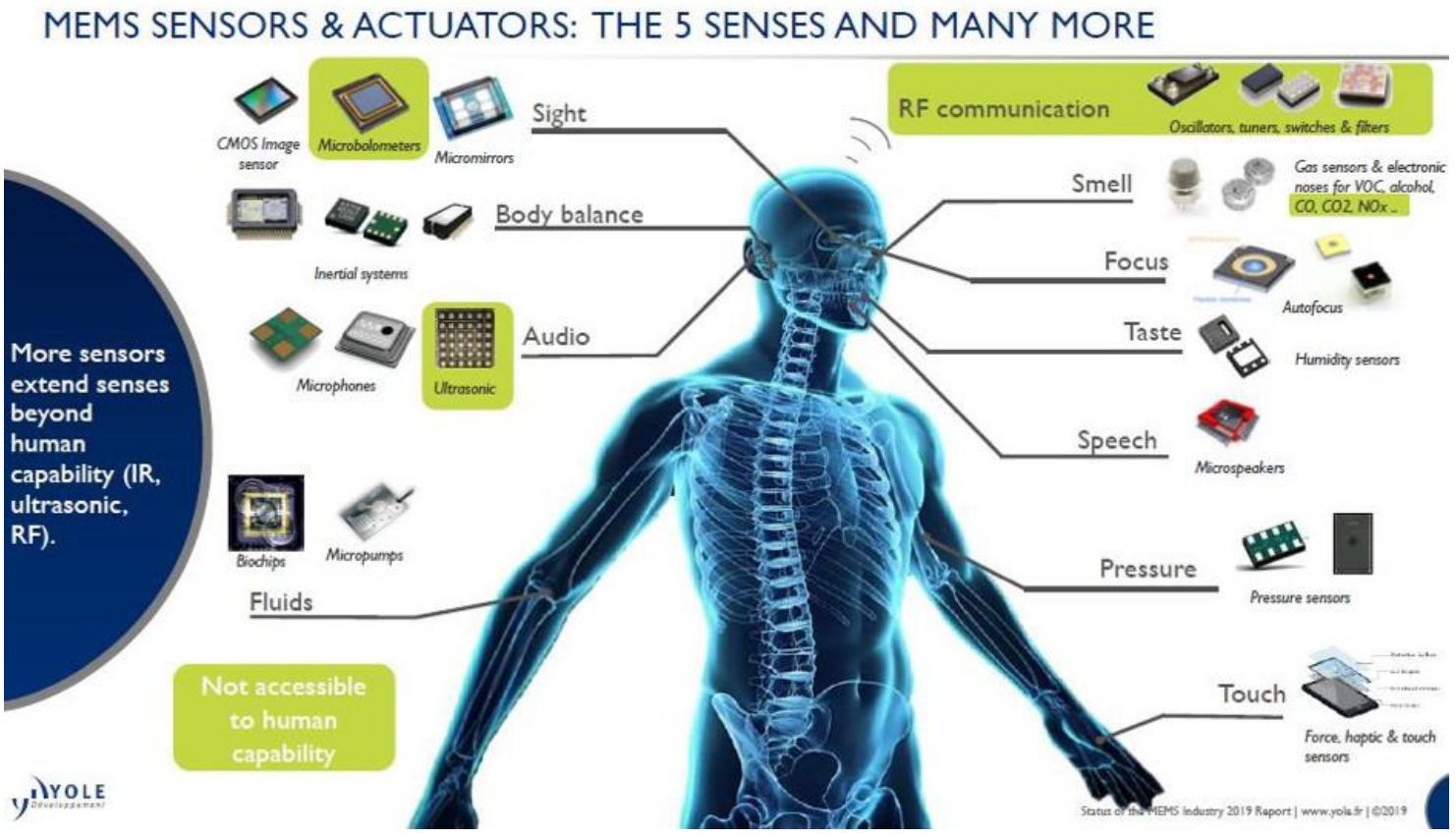
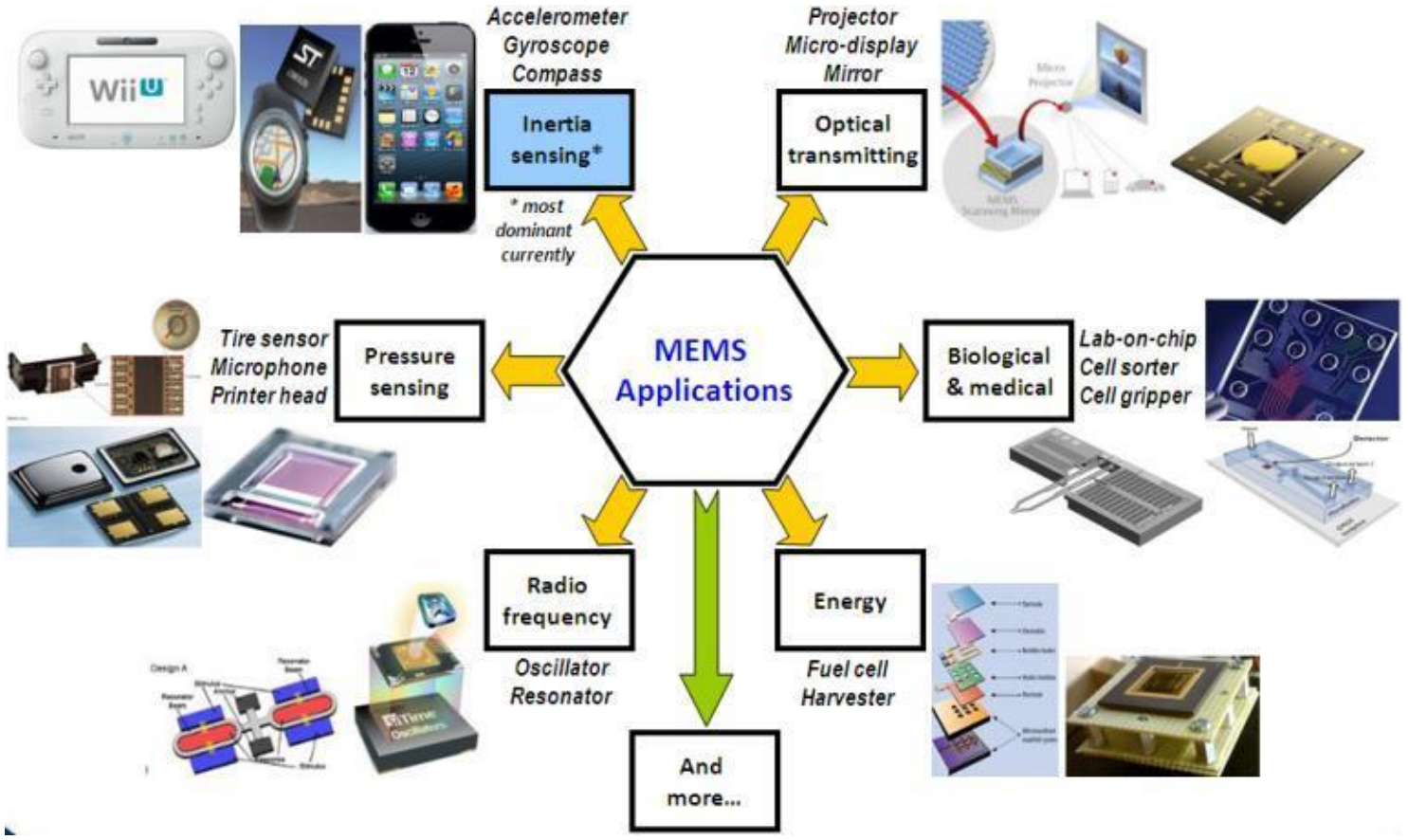


Image Credits: Yole

MEMS devices

- ~$17B market in 2018, growth at ~10% per year



•Image Credits: DOI: 10.1109/ECTC.2013.6575798

Summary and Prospects for the Future

- Silicon technology has driven the semiconductor industry for the last 50+ years
- Si CMOS is the basic toolset for many areas of science and engineering
- But, conventional Si technology is currently facing challenges (scaling, cost of production)
- Money challenge: Return on huge investment in fabs is limited
- Physics challenge: We are now entering the era of atomic dimensions -> device operation fundamentally different!
- Opportunity: We are on the cusp of a new semiconductor revolution!
- Many “More than Moore” technologies are emerging: photonics, spintronics, MEMS, etc.
- Along with other emerging materials, such as 1D and 2D materials and WBG semiconductors
- Simultaneously, engineers continue to tackle “More Moore” miniaturization with device innovations
- The semiconductor industry continues to grow and underpins our modern world
- Many exciting emerging opportunities…biosensing, quantum computing, sustainability, space exploration, and more we cannot even predict

Image Credits: AnySilicon, Wikipedia